Registration No.: | | | | | | | | | | |

Total Number of Pages: 03 **Course: B.Tech/IDD**
Sub_Code: EOPC2002

3rd Semester Regular Examination: 2024-25
SUBJECT: Analog and Digital Electronic Circuits
BRANCH(S): BIOMED, ELECTRICAL, ELECTRICAL & C.E, EE, EEE
Time: 3 Hours
Max Marks: 100
Q.Code: R488
Answer Question No.1 (Part-I) which is compulsory, any eight from Part-II and any two from Part-III.
The figures in the right hand margin indicate marks.

Part-I

Q1 **Answer the following questions:** **(2 x 10)**

a) Write the essentiality of DC Analysis and drawing DC load line for a semiconductor device like BJT. Explain, why the load line is a straight line and not a curve.

b) Define stability of a system. What are the stability factors? How the stability factors are related to stability of a system? For a fixed-bias configuration, what would be the value of current stability factor, if $\beta = 50$?

c) Explain why modelling is required while analyzing a BJT circuit? Draw the r_e model for transistor in common collector configuration.

d) With neat sketches, explain how the T-equivalent model of a MOSFET is developed?

e) Name the typical compound configurations of MOSFETs. How these compound configurations are useful in electronic circuits?

f) What is a positive feedback circuit? What are the mandate criteria for sinusoidal oscillation?

g) Differentiate between common amplifier and power amplifier circuits. How the power amplifiers are classified?

h) If 'A' numbers of 'B' bit parallel adders are required for a 16 x 8 Multiplier, then mention the values of 'A' and 'B'.

i) Draw a T-flip flop and write its excitation table.

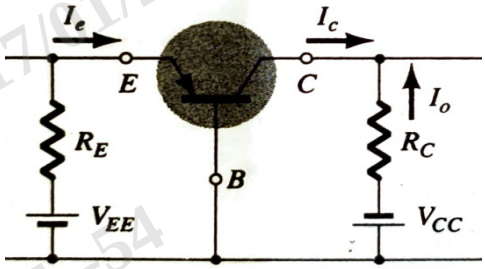
j) Explain Fan-in and Fan-out?

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 x 8)**

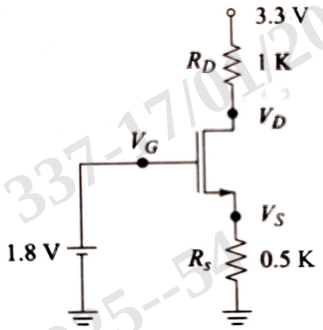
a) Explain the simplest form of self-bias circuit. Why it is named so? Determine V_{CEQ} and I_E for an emitter-biased emitter follower circuit having $\beta = 90$, $V_{CC} = 0V$, $V_{EE} = -20V$, $R_B = 240K\Omega$, $R_E = 2K\Omega$, and blocking capacitors = $10\mu F$.

b) Draw the approximate r_e model for a CB npn transistor. How it is different from the exact model? For the network with α = 0.98, V_{CC} = 8V, V_{EE} = 2V, R_E = 1KΩ, R_C = 5KΩ, r_O =1 MΩ, determine r_e, Z_i, Z_o, A_V, and A_i.



c) Determining the signal current in the drain terminal and voltage gain. Explain the small signal operation of MOSFET. Draw the equivalent model of a MOSFET by both neglecting and including the effect of channel length modulation.

d) What is the role of resistor R_S in biasing a MOSFET? The transistor in the following figure has V_T = 1V and $\mu_n C_{ox}(W/L)$ = 2 mA/V^2. Determine the drain voltage.



e) Explain the Wien bridge oscillator circuit finding feedback factor B and A. Discuss about its advantages and disadvantages. Write a note on crystal oscillator.

f) How the power amplifiers are classified? Explain the operation of class-A amplifier. Explain, how it is different from a class-B push-pull amplifier explaining the principle of operation and finding the power efficiency of it.

g) Minimize the following logic function using K-Maps and realize using universal gates. $F(A,B,C) = \bar{A}\,\bar{B}\,\bar{C} + A\,\bar{C}\,\bar{D} + A\bar{B} + ABC\bar{D} + \bar{A}\,BC$

h) Implement a half-adder with the help of a decoder. Realize the function F= x ⊕ y ⊕ z using 2:1 multiplexer only.

i) What is a flip-flop? Design a SR flip-flop using a JK flip-flop.

j) Differentiate between the asynchronous counter and synchronous counter. Design a 3-bit asynchronous up counter.

k) Draw and explain the working of bidirectional 5-bit shift register

l) The content of a 4-bit shift register is initially 1011. The register is shifted five times to the right with the serial input being 11010. Show the content of the register after each shift.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

Q3 What is meant by stability of a system? Determine the various stability factors of fixed bias and emitter bias configurations. Calculate the stability factor and the change in I_c from 25°C to 100°C for a silicon transistor defined by the following table for the emitter-bias arrangements. **(16)**

(a) $R_B = 250R_E$
(b) $R_B = 10R_E$
(c) $R_E = 100R_B$

$T\,(°C)$	$I_{co}\,(nA)$	β	$V_{BE}\,(V)$
−65	0.2×10^{-3}	20	0.85
25	0.1	50	0.65
100	20	80	0.48
175	3.3×10^{3}	120	0.3

Q4 A fixed-bias configuration of FET has an operating point V_{GSQ} = –2V and I_{DQ} = 5.625 mA, with I_{DSS} = 10mA and V_P = –6V. The value of y_{os} is given as 20µS. Determine g_m, r_d, Z_i, Z_0 with and without the effect of r_d, A_v with and without the effect of r_d. Explain the operation of a source follower circuit. Discuss about its various applications. What is the role of feedback resistor R_G in a network using drain to gate feedback biasing? For a voltage divider network, calculate the value of Z_i, Z_o, and V_o with V_{DD} = 18 V, R_1 = 91 MΩ, R_2 = 15 MΩ, R_D = 6.8 KΩ, and R_S = 3.3 KΩ. **(16)**

Q5 Explain the Positive feedback circuit as Oscillator. Write all about the R-C phase shift oscillator deriving the frequency of oscillation. Design a R-C phase shift oscillator for a frequency of 100 KHz assuming that h_{fe} = 100, h_{ie} = 1 KΩ, at V_{CE} = 5 V, I_C = 1 mA, and V_{CC} = 20 V. **(16)**

Q6 Differentiate a latch from a flip-flop. Explain the operation of a SR latch and a D flip-flop. Design a counter using JK flip-flops which counts the sequence: 0, 4, 2, 1, 6 and back to 0. Briefly explain the JK master-slave flip-flop. **(16)**